REMARKS/ARGUMENTS

The Office Action mailed September 16, 2005 has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

The 35 U.S.C. § 102 Rejection

Claims 1-37 stand rejected under 35 U.S.C. § 102(e) as being allegedly anticipated by Homewood et al (hereinafter Homewood).[1] This rejection is respectfully traversed.

According to the M.P.E.P., a claim is anticipated under 35 U.S.C. § 102(a), (b) and (e) only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.[2]

Claim 1

Regarding claim 1, the Office Action contends that Homewood teaches an apparatus for exception handling in a data packet processor (i.e., the data processor), comprising a packet processing pipeline (i.e., the instruction execution pipeline) including at least two processing stages for processing a sequential (i.e., each instruction passes sequentially through each pipeline stage in order to complete its execution) plurality of data packets (i.e., instructions), each of the plurality of data packets having an exception map (i.e., other than instruction bits in 128-bit wide words stored in the instruction cache) associated therewith, wherein the exception map has one or more entries, each of the entries associated with a particular exception condition; an exception detector (the interrupt and exception controller) associated with each of the processing stages, the

[1] U.S. Patent No. 6,807,628.
[2] Manual of Patent Examining Procedure (MPEP) § 2131. See also *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

detector detecting whether any of a plurality of exception conditions applies/associated to data packet; and a bit setter responsive to the exception detector to set, modify, or reset at least one of the entries (i.e., a valid stop bit) of an exception map associated with the data packet. The Office Action further contends that the further limitation of processing the execution map, by an exception handler, at a stage later than a stage in which the bit setter has set, monitored or reset one of the entries is an inherent feature, alleging that in the pipeline processing taught by Homewood, if one of the entries is set, modified or reset in a particular/current stage, then processing of that modification has to be handled/processed in the next/following stage. Applicants respectfully disagree for the reasons set forth below.

Homewood shows that an instruction cache 215 (Fig. 2) in a data processor that stores instructions, not data packets. Further, contrary to the Office Action, Homewood does not show that anything other than instruction is stored in the instruction cache and, specifically there is no "exception map" or equivalent thereof shown in Homewood. Further, Homewood neither expressly nor inherently describes processing data packet and an exception map associated with a data packet to deal with exception conditions in data packet transmission.

Further, while Homewood shows an interrupt and exception controller operative to detect an exception condition associated with one of the executing instructions and generate an exception in response to the execution condition upon completed execution of earlier ones of the executing instructions, and while Homewood further shows that instruction bundles have a valid stop bit, Homewood does not show that data packets have a bit associated with an exception condition, and thus does not show that each data packet has an exception map containing one or more bits/entries associated with exception conditions.

In contrast, claim 1 requires that each data packet has an associated exception map with one or more entries, each associated with a particular exception condition (page 8, line 22 - page 9, line 2 of the specification).

Further, Homewood shows that an interrupt and exception controller detects an exception condition associated with an executing instructions issued at time t_0 and generates an exception in response to the exception condition upon completed execution of ones of the executing instructions issued at the time preceding to t_0. Homewood does not show that where an exception condition is detected, a processing stage following to the stage at which the exception condition is detected is not started. In other words, Homewood does not show processing a detected exception condition at a stage later than a stage at which a bit is set, modified or reset upon the detection of the exception condition, and particularly, does not do so in conjunction with the processing of a data packet, which itself cannot be executed.

In contrast, in the present invention, detected exception conditions are not processed at each of the stages at which the exception conditions may be detected. Rather, the exception map are processed at a stage later than a stage at which, the bits are set or reset in the exception map in response to the detection of the exception conditions (page 10, line 22- page 12 line 2 of the specification).

Accordingly claim 1 is not anticipated by Homewood.

Claims 2

Regarding claim 2, the Office Action contends that Homewood teaches all the elements of base claim 1 and also teaches that each of the exception conditions further comprises a plurality of logical operations, i.e., the arithmetic or load/store operations. Applicants respectfully disagree for the reasons set forth below.

First of all, as to dependent claim 2, the argument set forth above is equally applicable here. The base claim 1 being allowable, the dependent claim 2 must also be allowable.

Further, Homewood shows that an arithmetic or load/store operation may be placed in any of the four words encoding the operations for a single cycle. However, Homewood does not show that the four words encoding the operations for a single cycle themselves contain an exception condition. Homewood neither expressly nor inherently describes that each of the exception conditions further comprises a plurality of logical operations. Accordingly, claim 2 is not anticipated by Homewood.

Claim 3

Regarding claim 3, the Office Action contends that Homewood teaches all the elements of base claim 1 and also teaches that the apparatus further comprising an exception handler to process the exception map in response to the entries that are set in the exception map when all of the processing stages are complete, i.e., by generating an exception in response to the exception condition upon completed execution of earlier ones of the executing instructions. Applicants respectfully disagree for the reasons set forth below.

First of all, as to dependent claim 3, the argument set forth above is equally applicable here. The base claim 1 being allowable, the dependent claim 3 must also be allowable.

Further, Homewood shows generating an exception in response to an exception condition when execution of one of the executing instructions, which were issued before the exception condition is detected, is complete. However, Homewood does not show processing one or more entries associated with a particular exception condition when all of the processing stages are complete. Further, Homewood neither expressly nor inherently shows that the exception handler

processes the exception map in response to the entries that are set in the exception map when all of the processing stages are complete. Accordingly, claim 3 is not anticipated by Homewood.

Claim 4

Regarding claim 4, the Office Action contends that Homewood teaches all the elements of base claim 1 and also teaches that the apparatus further comprising a memory (i.e., the instruction cache) associated with the data packet to store the exception map (i.e., other than instruction bits in 128-bit wide words stored in the instruction cache). Applicants respectfully disagree for the reasons set forth below.

First of all, as to dependent claim 4, the argument set forth above is equally applicable here. The base claim 1 being allowable, the dependent claim 4 must also be allowable.

Further, Homewood neither expressly nor inherently describes an apparatus further comprising a memory associated with the data packet to store the exception map. Accordingly, claim 4 is not anticipated by Homewood

Claims 8, 15, 22, 29, 31

The Office Action contends that the rejection of claim 1 is also applicable to claims 8, 15, 22, 29, 31. As to claims 8, 15, 22, 29, 31, the arguments set forth above are equally applicable here. For the same reasons as set forth with respect to claim 1, these claims are not anticipated.

Claims 6, 9, 13, 16, 20, 23, 27, 32, 36

The Office Action contends that the rejection of claim 2 is also applicable to claims 6, 9, 13, 16, 20, 23, 27, 32, 36. As to claims 6, 9, 13, 16, 20, 23, 27, 32, 36, the arguments set forth

above are equally applicable here. For the same reasons as set forth above with respect to claim 2, these claims are not anticipated.

Claims 5, 10, 12, 17, 19, 24, 26, 30, 33, 35

The Office Action contends that the rejection of claim 3 is also applicable to claims 5, 10, 12, 17, 19, 24, 26, 30, 33, 35. As to claims 5, 10, 12, 17, 19, 24, 26, 30, 33, 35, the arguments set forth above are equally applicable here. For the same reasons as set forth above with respect to claim 3, these claims are not anticipated.

Claims 7, 11, 14, 18, 21, 25, 28, 34, 37

The Office Action contends that all rejection stated in claim 4 is also applicable claims 7, 11, 14, 18, 21, 25, 28, 34, 37. As to claims 7, 11, 14, 18, 21, 25, 28, 34, 37 the arguments set forth above are equally applicable here. For the same reason as set forth above with respect to claim 4, these claims are not anticipated.

The 35 U.S.C. § 103 Rejection

Claims 1-37 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Homewood in view of Dean,[3] among which claims 1, 5, 8, 12, 15, 19, 22, 26, 29, 30, 31, and 35 are independent claims. This rejection is respectfully traversed.

According to the Manual of Patent Examining Procedure (M.P.E.P.),

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or

[3] U.S. Patent No. 5,544,342.

> suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure.[4]

Claim 1

Specifically, the Office Action contends that even if processing the execution map by an exception handler, at a stage later than a stage in which the bit setter has set, modified or reset one of the entries is not an inherent feature, Dean teaches this limitation of processing/handling the exception at the next stage/cycle to avoid irreparable changes to the processor's state and that it would have been obvious to one having ordinary skill in the art at the time of the invention to incorporate Dean into Homewood in order to support this limitation. Applicants respectfully disagree for the reasons set forth below.

First of all, as mentioned above, Homewood does not show data packets, each having an exception map, which has one or more entries associated with a particular exception condition and that the execution map is processed at a stage later than a stage in which the bit setter has set, modified, or reset one of the entries in the exception map. Dean does not show an arrangement wherein each data packet has an exception map which has one or more entries associated with a particular exception condition. Accordingly, Homewood in view of Dean fails to teach all the limitations of claim 1.

Further, Dean shows that a processor begins exception handling during only the next cycle to the external processor transfer cycle. However, Dean does not show handling exception conditions at any cycle/stage later than a cycle/stage in which an exception detector detects an exception condition regardless of the fact that an exception condition may be detected every stage/cycle (page 3, line 17 of the specification). Further, there is no suggestion or motivation to

[4] M.P.E.P § 2143.

combine Dean with Homewood, whether explicitly or implicitly in Dean or Homewood, or in the knowledge generally available to one of ordinary skill in the art at the time this invention was made. Accordingly, it would not have been obvious to a person skilled in the art to create the invention of claim 1.

Claim 2

Regarding dependent claim 2, the Office Action contends that the combination of Homewood and Dean teaches the claimed invention as described above and that Homewood teaches that each of the exception conditions further complies a plurality of logical operations, i.e. the arithmetic or load/store operations.

The arguments set forth above are equally applicable here. The base claim 1 being allowable, the dependent claim 2 must also be allowable. Dean adds nothing. Accordingly, claim 2 is not obvious.

Claim 3

Regarding dependent claim 3, the Office Action contends that the combination of Homewood and Dean teaches the claimed invention as described above and that Homewood teaches that the apparatus further comprising an exception handler to process the exception map in response to the entries that are set in the exception map when all of the processing stages are complete, i.e., by generating exception in response to the exception condition upon completed execution of earlier ones of the executing instructions.

The arguments set forth above are equally applicable here. The base claim 1 being allowable, the dependent claim 3 must also be allowable. Dean adds nothing. Accordingly, claim 3 is not obvious.

Claim 4

Regarding claim 4, the Office Action contends that the combination of Homewood and Dean teaches the claimed invention as described above and that Homewood teaches that the apparatus further comprises a memory (i.e., the instruction cache) associated with the data packet to store the exception map (other than instruction bits in 128-bit wide words stored in the instruction cache).

The arguments set forth above are equally applicable here. The base claim 1 being allowable, the dependent claim 4 must also be allowable. Dean adds nothing. Accordingly, claim 4 is not obvious.

Claims 8, 15, 22, 29, 31

The Office Action contends that the rejections stated above with respect to claim 1 also apply to claims 8, 15, 22, 29, 31. As to claims 8, 15, 22, 29, 31, the arguments set forth above are equally applicable here. Accordingly, claims 8, 15, 22, 29, 31 are not obvious.

Claims 6, 9, 13, 16, 20, 23, 27, 32, 36

The Office Action contends that the rejections stated above with respect to claim 2 also apply to claims 6, 9, 13, 16, 20, 23, 27, 32, 36. As mentioned above, claim 2 is allowable for the same reasons as stated for claim 1. As to claims 6, 9, 13, 16, 20, 23, 27, 32, 36, the arguments set forth above are equally applicable here. Accordingly, claims 6, 9, 13, 16, 20, 23, 27, 32, 36 are not obvious.

Claims 5, 10, 12, 17, 19, 24, 26, 30, 33, 35

The Office Action contends that the rejections stated above with respect to claim 3 also apply to claims 5, 10, 12, 17, 19, 24, 26, 30, 33, 35. As mentioned above, claim 3 is allowable for the same reasons as stated for claim 1. As to claims 5, 10, 12, 17, 19, 24, 26, 30, 33, 35, the arguments set forth above are equally applicable here. Accordingly, claims 5, 10, 12, 17, 19, 24, 26, 30, 33, 35 are not obvious.

Claims 7, 11, 14, 18, 21, 25, 28, 34, 37

The Office Action contends that the rejections stated above with respect to claim 4 also apply to claims 7, 11, 14, 18, 21, 25, 28, 34, 37. As mentioned above, claim 4 is allowable for the same reason as stated for claim 1. As to claims 7, 11, 14, 18, 21, 25, 28, 34, 37, the arguments set forth above are equally applicable here. Accordingly, claims 7, 11, 14, 18, 21, 25, 28, 34, 37 are not obvious.

In view of the foregoing, it is respectfully asserted that all rejections should be withdrawn and that all of the claims are now in condition for allowance.

Conclusion

It is believed that this Amendment places the above-identified patent application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case. Please charge any additional required fee or credit any overpayment not otherwise paid or credited to our deposit account No. 50-1698.

Respectfully submitted,

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